



Product Order Numbers

40G	XenaCompact: XenaBay:	C1-M2QSFP+ M2QSFP+
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Xena M2QSFP+

Gigabit Ethernet Test Module

The M2QSFP+ is a 2-port 40GBASE Quad Small Form-Factor Pluggable Plus (QSFP+) test module for our XenaCompact and XenaBay chassis. This module delivers a breakthrough price/performance benchmark for BERT, load-stress, and functional testing of Ethernet equipment and network infrastructure.

TOP FEATURES

- Supports QSFP+
- Price/performance
- Ease of use
- Free software (incl. XenaManager GUI, XenaIntegrator, XenaScripting, Xena2544, Xena1564, Xena3918, and Xena2889)
- Free 12-month hardware warranty
- 36 months free software updates
- Free tech support product lifetime



Broad range of applications

- Wire-speed hardware based traffic generation and analysis with full-line-rate Ethernet and IP packet generation at over 148 million packets per second
- Compatible with 40G QSFP+ compliant transceiver modules, using MPO connectors
- For lab testing, pre-staging, field trials and early deployments, and applications where wire-speed testing, portability, and ease of use are required
- Stream-based layer 2-3 traffic load generation for millions of flows, and for assessing layer 2-3 performance of 40 Gbit/s Ethernet equipment and services
- BERT functionality for verifying the integrity of 40 Gbit/s Ethernet running on WDM networks, at L2-3
- High-precision measurement of throughput, latency, loss, data integrity, inter-arrival time, sequence and mis-ordering errors
- Wire-speed traffic capture with programmable filter and trigger criteria, and export to industry standard tool WireShark
- Ability to adjust the parts per million Tx frequency over a range of +/-400 ppm
- Free software includes XenaManager, XenaScripting, Xena2544, Xena1564, Xena3918 and Xena2889 test suites
- Available for the XenaCompact chassis and the 12-slot XenaBay chassis for larger 40G port-counts



The M2QSFP+ test module supports 40Gbps QSFP+ transceivers and provides a comprehensive suite of test features for Layer 2 and Layer 3, including protocol testing, capture, histograms, service disruption measurements, multi-stream Ethernet generation & test and RFC 2544 and RFC 2889 benchmarking. This is augmented with 40G-specific features such as virtual lane swapping, skewing and PRBS testing.

Full-line-rate testing of Layer 2-3 performance of 40 Gbit/s Ethernet links is provided. The high precision, stream based, Layer 2-3 wire-speed traffic generation and analysis capabilities are suited for testing of network devices under deliberate error, stress, and random conditions. Packet formats can be defined per individual

packet byte, and packet spacing, transmission rates, and bursts can be defined with byte and kbps accuracy.

Ethernet is increasingly carried across a variety of layer 1 media over longer distances, which creates a need for the characterization of Ethernet transport on a bit-per-bit basis. The bit-error-rate testing (BERT) function uses a pseudo-random binary sequence (PRBS) encapsulated into an Ethernet frame, making it possible to go from a frame-based error measurement to a bit-error-rate measurement. This provides the bit-per-bit error count accuracy required for the characterization and acceptance testing of physical-medium transport systems such as Ethernet-over-DWDM.

SPECIFICATIONS

PORT LEVEL FEATURES	40G
Product Order Numbers	XenaCompact: C1-M2QSFP+ XenaBay: M2QSFP+
Interface category	40G Ethernet (2 x 40GBASE-SR4 / 1 X 40GBASE-LR4)
Number of test ports (software configurable)	2 x 40G
Number of transceiver module cages	2 x QSFP+
Port statistics ²⁾	Link state, FCS errors, pause frames, ARP/PING, error injections, training packet All traffic: RX and TX Mbit/s, packets/s, packets, bytes Traffic w/o test payload: RX and TX Mbit/s, packets/s, packets, bytes
Adjustable Inter Frame Gap (IFG)	Configurable from 16 to 56 bytes, default is 20B (12B IFG + 8B preamble)
Transmit line rate adjustment	Ability to adjust effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 0.001 ppm (shared across all ports)
ARP/PING	Supported (configurable IP and MAC address per port)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and Software)
Tx disable	Enable/disable of optical laser or copper link
IGMPv2 multicast join/leave	IGMPv2 continuous multicast join, with configurable repeat interval
Histogram statistics ²⁾	Two real-time histograms per port. Each histogram can measure one of RX/TX packet length, IFG, or Latency distribution for all traffic, a specific stream, or a filter
Loopback modes	<ul style="list-style-type: none"> L1RX2TX (RX-to-TX, transmit byte-by-byte copy of the incoming packet) L2RX2TX (RX-to-TX, swap source and destination MAC addresses) L3RX2TX (RX-to-TX, swap source and destination MAC addresses and IP addresses) TXON2RX (TX-to-RX, packet is also transmitted from the port) TXOFF2RX (TX-to-RX, port's transmitter is idle)

TRANSMIT ENGINES	
Number of transmit streams per port	64 (wire-speed) Each stream can generate millions of traffic flows through the use of field modifiers
Test payload insertion per stream	Wire-speed packet generation with timestamps, sequence numbers, and data integrity signature optionally inserted into each packet.
Stream statistics ²⁾	TX Mbit/s, packets/s, packets, bytes, FCS error, Pause
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved.
Field modifiers	16-bit header field modifiers with inc, dec, or random mode. Each modifier has configurable bit-mask, repetition, min, max, and step parameters. 2 modifiers per stream
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions (from 56 to 9200 bytes)
Packet payloads	Repeated user specified 1 to 18B pattern, a 8-bit incrementing pattern
Error generation	Undersize length (56B min) and oversize length (9200 max.) packet lengths, injection of sequence, misorder, payload integrity, and FCS errors
TX packet header support and RX autodecodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	<ul style="list-style-type: none"> Normal (stream interleaved mode). Standard scheduling mode, precise rates, minor variation in packet inter-frame gap. Strict Uniform. New scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream



RECEIVE ENGINE

Number of traceable Rx streams per port	480 (wire-speed)
Automatic detection of test payload for received packets	Real-time reporting of statistics and latency, loss, payload integrity, sequence error, and disorder error checking
Jitter measurement	Jitter (Packet Delay Variation) measurements compliant to MEF10 standard with 8 ns accuracy
Stream statistics ²⁾	<ul style="list-style-type: none"> • RX Mbit/s, packets/s, packets, bytes. • Loss, payload integrity errors, sequence errors, disorder errors • Min latency, max latency, average latency • Min jitter, max jitter, average jitter
Latency measurements accuracy	±16 ns
Latency measurement resolution	8 ns (<i>Latency measurements can calibrate and remove latency from transceiver modules</i>)
Number of filters:	<ul style="list-style-type: none"> • 4 x 64-bit user-definable match-term patterns with mask, and offset • 4 x frame length comparator terms (longer, shorter) • 4 x user-defined filters expressed from AND/OR'ing of the match and length terms.
Filter statistics ²⁾	Per filter: RX Mbit/s, packets/s, packets, bytes.

CAPTURE

Capture criteria	All traffic, stream, FCS errors, filter match, or traffic without test payloads
Capture start/stop triggers	Capture start and stop trigger: none, FCS error, filter match
Capture limit per packet	16 – 9200 bytes
Wire-speed capture buffer per port	256 kB
Low speed capture buffer per port (10Mbit/s speed)	4096 packets (any size)

40G FRAMED BERT AND PCS LAYERS

Payload Test pattern	PRBS 2 ³¹
Error Injection	Manual single shot bit-errors or bursts, automatic continuous error injection
Frame size and header	Fixed size from 56 to 9200 bytes, any layer 2/3/4 frame header
Alarms	Pattern loss, bit-error rate threshold
Error analysis	bit-errors: seconds, count, rate mismatch '0' / '1': seconds, count, rate logging and analysis of bit-error event timing
PCS virtual lane configuration	User defined skew insertion per Tx virtual lane, and user defined virtual lane to SerDes mapping for testing of the Rx PCS virtual lane re-order function.
PCS virtual lane statistics	Relative virtual lane skew measurement (up to 2048 bits), sync header and PCS lane marker error counters, indicators for loss of sync header and lane marker, BIP8 errors
PCB Tx line clock adjustment (FCO)	Ability to adjust the parts per million (ppm) Tx frequency over a range of -400 to +400 ppm

1) Requires Reflex Photonics CFP 100GBASE-SR10 Parallel Optical Module

2) Counter size: 64 bits

PHYSICAL

1U XenaCompact

- W: 19" (48.26 cm)
- H: 1.75" (4.45 cm)
- D: 9.8" (25 cm)
- Weight: 10 lbs (4.5 kg)

4U XenaBay

- W: 19" (48.26 cm)
- H: 7" (17.78 cm)
- D: 19.7" (50 cm)
- Weight: 36.4 lbs (16.5 kg)

ENVIRONMENTAL

- Operating Temperature: 10 to 35° C
- Storage Temperature: -40 to 70° C
- Humidity: 8% to 90% non-condensing

POWER

- AC Voltage: 100-240V
- Frequency: 50-60Hz
- Max. Power: 30W for M2QSFP+ (90W XenaCompact / 120W XenaBay)
- Max. Current: 0.8A with 120V supply, and 0.4A with 240V supply

REGULATORY

FCC (US), CE (Europe)



Xena Networks is an award-winning manufacturer of advanced Gigabit Ethernet test and measurement solutions.



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